WHAT IS CLAIMED IS:

1. An electrostatic discharge (ESD) protection circuit, comprising:

a silicon controlled switch (SCS) installed between positive and negative power supply nodes;

a switch control circuit installed between the positive power supply terminal and the gate of the silicon controlled switch (SCS);

a metal oxide semiconductor field effect transistor (MOSFET) connected to a transistor emitter in the silicon controlled switch (SCS) to cause the silicon controlled switch (SCS) to be triggered into conduction; and

a transistor control circuit installed between the positive power supply terminal and the metal oxide semiconductor field effect transistor (MOSFET);

whereby when the forward over-voltage stress occurs over the positive power supply terminal in the active mode, the transistor control circuit can be enabled to turn on the metal oxide semiconductor field effect transistor (MOSFET), and at the same time the switch control circuit can be enabled to trigger the silicon controlled switch (SCS) into conduction to form a discharging path, such that the terminal voltage over the positive power supply terminal will be rapidly decreased to the level of a holding voltage of the silicon controlled switch (SCS) to provide ESD protection and prevent latch-up of the silicon controlled switch (SCS).

2. The ESD protection circuit as claimed in claim 1, wherein the silicon controlled switch (SCS) is formed by an NPN transistor and a PNP transistor, wherein a first anode of the SCR is formed by an emitter of the PNP transistor, and a second anode of the SCR is formed by a base of the PNP transistor which is

connected to the positive power supply terminal through a resistor R_N, and a cathode is formed by a collector of the PNP transistor which is connected to a base of the NPN transistor and further through a resistor R_{SUB} to the ground terminal, and a gate is formed by the base of the PNP transistor which is connected to a collector of the NPN transistor.

3. The ESD protection circuit as claimed in claim 1, the transistor control circuit is formed by a capacitor and a resistor, and the capacitor-resistor node is connected to the gate of the metal oxide semiconductor field effect transistor (MOSFET), such that a time constant of the circuit can be determined by adjusting the values of the capacitor and the resistor, so as to control the conduction time of the metal oxide semiconductor field effect transistor (MOSFET).

4 The ESD protection circuit as claimed in claim 2, wherein the switch control circuit has a Zener diode connected across the base electrodes of complementary PNP/NPN transistors in the silicon controlled switch (SCS), so that a discharge current can continue after the metal oxide semiconductor field effect transistor (MOSFET) is disabled.

5. The ESD protection circuit as claimed in claim 4, wherein the Zener diode of the switch control circuit is connected in series by a diode.

6. The ESD protection circuit as claimed in claim 2, wherein the silicon controlled switch (SCS) is connected to the ground terminal through a diode array in series.

7. The ESD protection circuit as claimed in claim 6, wherein the metal oxide semiconductor field effect transistor (MOSFET) is connected between the

silicon controlled switch (SCS) and the ground terminal through a drain and a source, and the gate is coupled to the transistor control circuit.

8. The ESD protection circuit as claimed in claim 2, wherein the silicon controlled switch (SCS) is connected to the positive power supply terminal through a diode array in series.

9. The ESD protection circuit as claimed in claim 8, wherein the metal oxide semiconductor field effect transistor (MOSFET) is connected between the positive power supply terminal and the silicon controlled switch (SCS) through a drain and a source, and the gate is coupled to the transistor control circuit.

10. The ESD protection circuit as claimed in claim 2, wherein the switch control circuit has a NMOS transistor connected across the base electrodes of complementary PNP/NPN transistors in the silicon controlled switch (SCS).

11. The ESD protection circuit as claimed in claim 1, wherein the silicon controlled switch (SCS) is formed by an NPN transistor and a PNP transistor, wherein a first anode of the SCR is formed by an emitter of the NPN transistor, and a second anode of the SCR is formed by a base of the NPN transistor which is connected to the negative power supply terminal through a resistor R_N, and a cathode is formed by a collector of the NPN transistor which is connected to a base of the PNP transistor, and a gate of the SCR is formed by the base of the NPN transistor which is connected to a collector of the PNP transistor.